19. Write and verify an HDL behavioral description of the JK flip-flop using an if-else statement based on the value of the present state.

(a) Obtain the characteristic equation when $Q = 0$ or $Q = 1$.

(b) Specify how the J and K inputs affect the output of the flip-flop at each clock tick

20. Explain the design procedure of asynchronous sequential circuits.

APRIL/MAY 2025

FEEL64B/CEEL62B/BEEL62B — DIGITAL SYSTEM DESIGN

Time : Three hours Maximum : 75 marks

SECTION A — ($10 \times 2 = 20$ marks)

Answer ALL questions.

1. State Boolean commutative law.
2. Give the truth table of Not gate.
3. What are called combinational circuits?
4. Define HDL.
5. What is an encoder?
6. What is 2:1 multiplexer?
7. What is race condition?
8. What is ring counter?
9. State the need of asynchronous circuit.
10. What is steady-state condition?

Shanmuga Industries Arts & Science College T.V.Malai

SECTION B — (5 × 5 = 25 marks)

Answer ALL questions.

11. (a) Describe Boolean theorems.

Or

(b) Explain all the logic gates.

12. (a) Describe the combinational circuit with neat block diagram.

Or

(b) How does the circuit for arithmetic operations can be done in combinational circuit?

13. (a) Elucidate the working of priority encoder.

Or

(b) Design a BCD-to-decimal decoder.

14. (a) Enumerate the functioning of D Latch.

Or

(b) Write and verify the HDL behavioral description of a four-bit shift register.

Shanmuga Industries Arts & Science College T.V.Malai

15. (a) Outline the analysis procedure of asynchronous sequential circuits.

Or

(b) Write a short note on race free state assignment.

SECTION C — (3 × 10 = 30 marks)

Answer any THREE questions.

16. Simplify the following Boolean functions using Karnaugh map

Y = A'B'CD + A'BCD + ABCD + AB'CD + ABC'D' + ABC'D + ABCD'

17. Explain the analysis procedure of combinational circuits.

18. Write the HDL dataflow description of a quadruple 2-to-I-line multiplexer with enable.